## REMARKS

The present invention relates to a wiring substrate and a process for producing a wiring substrate which, *inter alia*, employs a particular embedding resin.

In the Office Action dated June 4, 2003, the Examiner suggested some possible amendments to claims 7 and 8. Claims 1, 2, 4, 5, 8, and 9 were rejected under 35 U.S.C. § 102(b) based on Kawamoto et al, and claims 1-5, 8 and 9 were rejected under 35 U.S.C. § 102(e) based on Nakamura et al. Claim 7 was rejected under 35 U.S.C. § 103(a) based on Kawamoto et al. Lastly, it is appreciated that the Examiner indicated that claim 6, although objected to as being dependent upon a rejected base claim, would be allowable if rewritten in independent form, particularly in view of the Examiner's stated recognition that although Kawamoto et al disclosed an outer wiring connection that can act as an electrode, Kawamoto et al does not teach or disclose the instantly claimed roughened surface.

First, in response to the Examiner's suggestions, claim 8 has been amended in accordance with the Examiner's suggestion. Claim 7 has been amended by the amendment of claim 4, on which claim 7 depends.

It is appreciated that the Examiner has recognized the fundamental patentability with respect to the subject matter set forth in claim 6, and has recognized that the subject matter set forth in claim 7 is not anticipated by the Kawamoto et al or Nakamura et al references.

In the above amendments to the claims, wiring substrate claim 4 has been amended to independent form, incorporating the recitation of cancelled claim 1 as well as the recitation of claim 6, which has accordingly been cancelled.

Similarly, independent process claim 9 has been amended to incorporate the recitation of cancelled claim 6.

Still further, new claim 10 has been set forth directed to a wiring substrate comprising further detailed features including the features set forth in claim 7 as well as the further requirement that the semiconductor is connected to the electronic part through a via hole penetrating the built-up layer provided between the semiconductor and electronic part (supported by the disclosure in this specification, for example, at page 23, lines 6-16).

In view of the foregoing, and considering, *inter alia*, that independent wiring substrate claim 4 and independent process claim 9 include the features of claim 6, which the Examiner has recognized are not disclosed in the prior art, and also considering the further features recited in independent wiring substrate claim 10, it is respectfully submitted that all of the independent and

dependent claims are patentable over the cited art of record, and are presently in condition for immediate allowance.

In view of the above, reconsideration and allowance of this application, including all of pending claims 2-5 and 7-10, is respectfully submitted to be proper. Such action is hereby earnestly solicited.

If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the local Washington D.C. telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Joseph J. Ruch, Jr.
Registration No. 26,577

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
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CUSTOMER NUMBER

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